L Number	Hits	Search Text	DB	Time stamp
3	0	((etch near3 stop) same (picvd)) and (opening or trench or recess or aperture or hole) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:22
4	178	((etch near3 stop) same (pecvd)) and (opening or trench or recess or aperture or hole) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:27
5	0	((etch near3 stop) same (picvd)) and (opening or trench or recess or aperture or hole) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:28
6	0	((etch near3 stop) same (photo adj induced)) and (opening or trench or recess or aperture or hole) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:35
7	0	((etch near3 stop) same (photo adj induced) same (silicon adj nitride)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:36
8	0	((etch near3 stop) same (picvd) same (silicon adj nitride)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:36
9	0	((picvd) same (silicon adj nitride)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:37
10	3	((photo adj induced) same (silicon adj nitride)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:38
11	74	((photo adj induced) with deposition) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:47
12	52	(((photo adj induced) with deposition) and @ad<19990903) and (stop or nitride)	USPAT; US-PGPUB	2004/11/17 16:38
13	4	(picvd same (dielectric or nitride)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 16:59
14	28	((photo adj induced) with deposition)	EPO; JPO; DERWENT; IBM_TDB	2004/11/17 16:48
15	7	(((photo adj induced) with deposition)) and (nitride or oxide or dielectric)	EPO; JPO; DERWENT; IBM_TDB	2004/11/17 16:49
16	11	((picvd) with deposition)	EPO; JPO; DERWENT; IBM_TDB	2004/11/17 16:49
17	2	(((picvd) with deposition)) and (nitride or oxide or dielectric)	EPO; JPO; DERWENT; IBM_TDB	2004/11/17 16:49
18	244	((picvd or (photo adj induced)) same (dielectric or nitride or oxide or insulating or insulative or insulator)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 17:01
19	125	((picvd or (photo adj induced)) with (dielectric or nitride or oxide or insulating or insulative or insulator)) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 17:01

L Number	Hits	Search Text	DB	Time stamp
1	2367	selectivity same opening	USPAT; US-PGPUB	2004/11/17 14:57
2	33	(selectivity same opening) and (air near3 gap)	USPAT; US-PGPUB	2004/11/17 14:59
3	22684	opening and (air near3 gap)	USPAT; US-PGPUB	2004/11/17 14:59
4	1852	(opening and (air near3 gap)) and etching	USPAT; US-PGPUB	2004/11/17 14:59
5	218	((opening and (air near3 gap)) and etching) and void	USPAT; US-PGPUB	2004/11/17 15:00
6	103	(((opening and (air near3 gap)) and etching) and void) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 15:06
7	70	((etch near3 stop) same air) and (opening or trench or recess or aperture or hole) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 15:16
8	180	((etch near3 stop) same (gap or void)) and (opening or trench or recess or aperture or hole) and @ad<19990903	USPAT; US-PGPUB	2004/11/17 15:12
9	153	(((etch near3 stop) same (gap or void)) and (opening or trench or recess or aperture or hole) and @ad<19990903) not (((etch near3 stop) same air) and (opening or trench or recess or aperture or hole) and @ad<19990903)	USPAT; US-PGPUB	2004/11/17 15:10
11	36	((etch near3 stop) same (gap or void)) and (opening or trench or recess or aperture or hole)	EPO; JPO; DERWENT; IBM_TDB	2004/11/17 15:12
12	2	((etch near3 stop) same air) and (opening or trench or recess or aperture or hole) and @ad<19990903	EPO; JPO; DERWENT; IBM_TDB	2004/11/17 15:16

DERWENT-ACC-NO: 2000-578983

DERWENT-WEEK: 200301

TITLE: Semiconductor device manufacturing method, involves forming of **void** between interconnections and **etch stop** **recess** portion over the **void** to prevent metal deposition in **void**

---------- KWIC ---------

Basic Abstract Text - ABTX (1):
NOVELTY - Semiconductor device manufacturing method involves depositing **etch** **stop** layer over dielectric layer (210) having crest portion and **recess** portion (217) over the interconnectors (206,208), and **void** (216) over a dielectric layer (204) on a substrate (202). The **stop etch** layers are planarized to obtain planar surface with **etch stop recess** portion (220) over the **recess** portion.

Basic Abstract Text - ABTX (2):
DETAILED DESCRIPTION - Semiconductor device manufacturing method involves selective etching of the conductive layer to form interconnects with a gap between them over a dielectric layer on a substrate (202). The void is formed in the gap by depositing a dielectric layer (210), having crest and **recess** portions over the interconnects and gap, respectively.

Basic Abstract Text - ABTX (4):
ADVANTAGE - Cross talk between the interconnects are

reduced by providing
void which reduces capacitance between interconnections.
The metal deposition
in **void** is prevented by **etch stop recess** portion.

Basic Abstract Text - ABTX (10):
Recess portion 217

Basic Abstract Text - ABTX (11):
Etch stop **recess** portion 220

Title - TIX (1):
Semiconductor device manufacturing method, involves
forming of **void** between
interconnections and **etch stop recess** portion over the **void**
to prevent metal
deposition in **void**

Equivalent Abstract Text - ABEQ (1):
NOVELTY - Semiconductor device manufacturing method
involves depositing **etch**
stop layer over dielectric layer (210) having crest portion
and **recess** portion
(217) over the interconnectors (206,208), and **void** (216)
over a dielectric
layer (204) on a substrate (202). The **stop etch** layers are
planarized to
obtain planar surface with **etch stop recess** portion (220)
over the **recess**
portion.

Equivalent Abstract Text - ABEQ (2):
DETAILED DESCRIPTION - Semiconductor device
manufacturing method involves
selective etching of the conductive layer to form
interconnects with a gap
between them over a dielectric layer on a substrate (202).
The void is formed
in the gap by depositing a dielectric layer (210), having
crest and **recess**
portions over the interconnects and gap, respectively.

Equivalent Abstract Text - ABEQ (4):
ADVANTAGE - Cross talk between the interconnects are reduced by providing
void which reduces capacitance between interconnections. The metal deposition
in **void** is prevented by **etch stop recess** portion.

Equivalent Abstract Text - ABEQ (10):
Recess portion 217

Equivalent Abstract Text - ABEQ (11):
Etch stop **recess** portion 220

Standard Title Terms - TTX (1):
SEMICONDUCTOR DEVICE MANUFACTURE METHOD FORMING **VOID** INTERCONNECT **ETCH STOP**
RECESS PORTION **VOID** PREVENT METAL DEPOSIT **VOID**

US-PAT-NO: 6190966

DOCUMENT-IDENTIFIER: US 6190966 B1

TITLE: Process for fabricating semiconductor memory device with high data retention including silicon nitride etch stop layer formed at high temperature with low hydrogen ion concentration

---------- KWIC ---------

Abstract Text - ABTX (1):

A semiconductor memory device such as a flash Electrically Erasable Programmable Read-Only Memory (Flash EEPROM) includes a floating gate with high data retention. A tungsten damascene local interconnect structure includes a silicon nitride etch stop layer which is formed using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) at a temperature of at least 480.degree. C. such that the etch stop layer has a very low concentration of hydrogen ions. The minimization of hydrogen ions, which constitute mobile positive charge carriers, in the etch stop layer, minimizes recombination of the hydrogen ions with electrons on the floating gate, and thereby maximizes data retention of the device.

Brief Summary Text - BSTX (18):

A tungsten damascene local interconnect structure includes a silicon nitride etch stop layer which is formed using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) at a temperature of at least 480.degree. C. such that the etch stop layer has a very low concentration of hydrogen ions.

Detailed Description Text - DETX (11):
FIG. 3 illustrates how a silicon nitride (S.sub.3 N.sub.4) etch stop layer 20 is formed over the surface 12a of the substrate 12 and the devices 14 in accordance with the present invention. The etch stop layer 20 is preferably formed using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) at a temperature of at least approximately 480.degree. C. to a thickness of approximately 800.+-.50 .ANG..

Claims Text - CLTX (4):
(c) forming a silicon nitride etch stop layer over the surface of the substrate and the device using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) at a temperature of at least approximately 480.degree. C., wherein step (c) comprises forming the etch stop layer using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) with:

Claims Text - CLTX (27):
12. A process as in claim 1, in which step (c) further comprises forming the etch stop layer with a spacing between a **PECVD** shower head and the surface of the substrate of approximately 9.5 millimeters.

Claims Text - CLTX (32):
(c) forming a silicon nitride layer over the surface of the substrate and the device using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) at a temperature of at least approximately 480.degree. C., wherein step (c) comprises forming the etch stop layer using Plasma Enhanced Chemical Vapor Deposition (**PECVD**) with:

US-PAT-NO: 5062508

DOCUMENT-IDENTIFIER: US 5062508 A

TITLE: CVD coating process for producing coatings and apparatus for carrying out the process

---------- KWIC ---------

Abstract Text - ABTX (1):

A plasma or **photo-induced** chemical vapor deposition coating process and apparatus are provided for applying thin dielectric coatings on planar, curved, and large area substrates. A plasma is generated in a tubular outer conductor. This plasma or the UV radiation occurring in the plasma passes through an opening into a reaction chamber. The opening preferably extends axially along the outer conductor and communicates with the interior of the reaction chamber. At least one component of the reaction gas is introduced directly to the opening or into the reaction gas is introduced directly to the opening or into the reaction chamber adjacent to the opening, bypassing the outer conductor. In this apparatus, the reactive deposition of a coating onto a substrate occurs only in the reaction chamber and below the opening from the outer conductor.

US-PAT-NO: 5660895

DOCUMENT-IDENTIFIER: US 5660895 A

TITLE: Low-temperature plasma-enhanced chemical vapor deposition of silicon oxide films and fluorinated silicon oxide films using disilane as a silicon precursor

---------- KWIC ---------

Brief Summary Text - BSTX (9):

The following papers discuss **photo-induced** chemical vapor **deposition** of silicon dioxide films using disilane: Y. Matsui et al., "Low-temperature Growth of SiO.sub.2 Thin Film by **Photo-Induced** Chemical Vapor **Deposition** Using Synchrotron Radiation," Jpn. J. Appl. Phys., vol. 31, pp. 1972-1978 (1992); K. Inoue et al., "Low Temperature Growth of SiO.sub.2 Thin Film by Double-Excitation Photo-CVD," Jpn. J. Appl. Phys., vol. 26, pp. 805-811 (1987); K. Inoue et al., "Growth of SiO.sub.2 Thin Film by Selective Excitation Photo-CVD Using 123.6 nm VUV Light," Jpn. J. Appl. Phys., vol. 27, pp. L2152-L2154 (1988); and M. Tsuji et al., "Deposition of SiO.sub.2 Film from ArF Laser Photolysis of Si.sub.2 H.sub.6 /N.sub.2 O Mixtures in a Parallel Irradiation Configuration," Jpn. J. Appl. Phys., vol. 32, pp. 139-143 (1993).

Other Reference Publication - OREF (16):

Y. Matsui et al., "Low-temperature Growth of SiO.sub.2 Thin Film by **Photo-Induced** Chemical Vapor **Deposition** Using Synchrotron Radiation," Jpn. J.

Appl. Phys., vol. 31, pp. 1972-1978 (1992).